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### REMARKS

In response to the filing of Applicants' Brief on Appeal, the Examiner withdrew many of the previous grounds of rejection, re-opened prosecution, and instituted several new grounds of rejection against pending claims 21-25 and 31-32. Applicants note that the latest Office Action is at least the tenth substantive action issued by the Examiner over a period of almost seven years. This responsive amendment represents an earnest attempt by applicants to advance prosecution and place all remaining claims in condition for allowance.

Basis for the amendments to the claims may be found in the specification at page 8, lines 31-32 ("overlayer 28 is much thicker than conductive layer 26") and page 6, lines 16-17, along with drawing figures 6 and 7 ("eliminates the risk of etching the contact hole through the conductive layer").

In the Office Action, the Examiner rejected claims 21, 22, 23, and 25 under 35 USC §102(e) as anticipated by Jost et al (US5563089). Jost teaches a method for forming a semiconductor device which, as illustrated in Figs. 9-12, involves etching an opening to a depth which completely etches through layer 44a as well as conductive layer 40 in the opening (see, Fig. 11). Claim 21, as presently amended, recites that the contact hole is etched in the overlayer and in an overetch amount that extends into but not through the conductive layer in the opening. As taught in applicants' specification, features of embodiments of the present invention include overetching of the contact hole into a locally thick region of the conductive layer, thus, "eliminate[ing] the risk of etching the contact hole through the conductive layer, improve[ing] the conductive layer/conductor contact, and prevent[ing] current leakage between the conductor and the substrate or other structure underlying the conductive layer." Jost does not teach or suggest a method as recited in amended claim 21. Accordingly, applicants request that this rejection, as well as the rejection of dependent claims 22-25, be withdrawn.

Also in the Office Action, the Examiner rejected claims 21-25, 31, and 32 under 35 USC §102(e) as anticipated by Jun (US5459094). The Examiner relied upon certain embodiments of Jun (see, Figs. 4a-4f) which depict forming a conductive layer 16 in a contact hole 15, followed by the deposition of an insulating layer 17 over conductive layer 16. After application of a photoresist mask, portions of layer 17 are etched, the etching continuing into conductive layer 16. However, Jun clearly depicts that layer 16 is much thicker than layer 17. Claims 21-25 and

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31-32, as presently amended, recite a process that includes forming an overlayer over a layer of conductive material on an underlayer, the overlayer having a thickness greater than the underlayer. Jun does not teach nor suggest such a method. Accordingly, applicants request that this rejection be withdrawn as Jun does not teach each and every limitation of the amended claims.

Also in the Office Action, the Examiner rejected claims 21-22, 24, and 31-32 under 35 USC §103 as unpatentable over Bergemont (US5484741) in view of Toshiyuki et al (JP-05-109905) and Zamanian (US5793111). Bergemont describes a method of making an increased density flash EPROM device. As shown in Figs 10, 12, 13, and 14, which are relied upon by the Examiner, Bergemont shows the formation of a "second oxide layer 118" over semiconductor substrate 102. As shown in Figs. 10 and 12, depending on the location, second oxide layer 118 is then either partially removed to leave oxide spacers 119 over an N<sup>+</sup> drain, or is left intact (see area above portion labeled common source bit line (CSBL) in Fig. 12. At no time during further processing is oxide layer 118 etched away.

Independent claims 21 and 31 recite "forming an underlayer having an opening over the at least one semiconductor layer" (claim 21) or "forming a structure having an opening in said at least one semiconductor layer" (claim 31). The Examiner asserted, page 4 of office action) that Bergemont taught forming an underlayer having an opening over the at least one semiconductor layer 102, asserting that "the underlayer is the remaining portion of the second oxide underlayer 118 located above the 'Source' after removing the photoresist." This assertion is factually incorrect.

The passages in Bergemont spanning columns 8 and 9 indicate that portions of second oxide layer 118 are protected by photoresist mask 120, while other portions are not. The portions that are removed constitute those areas of the device in which only oxide spacers 119 remain. During that removal (etch), other portions of second oxide layer remain protected. See, Fig. 11 and accompanying text at column 8, lines 56-67 and column 9, lines 1-22. Specifically, Bergemont teaches at column 9, lines 13-22, mask 120 is positioned to insure "that none of the layer of second oxide 118 formed over the common source bit lines CSBLs is removed during the etching step."

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Thus, the only "opening" formed in Bergemont's "underlayer" is one in which there is no later contact hole formed (left side of Figs. 10, 12, and 13-14). Also, that portion of oxide layer 118 that is beneath the later formed contact hole and plug 126 (right side of Figs. 10, 12, and 13-14) remains unaffected and is **continuous**; no hole is formed at that location. Accordingly, Bergemont fails to teach or suggest the subject matter recited in claims 21-22, 24, and 31-32. Any proposed combination of Bergemont with either Toshiyuki or Zamanian fails to cure the primary deficiency of Bergemont. The rejection of claims 21-22, 24, and 31-32 on this basis is not well taken and should be withdrawn.

Also in the Office Action, the Examiner rejected claims 21-25, and 31-32 under 35 USC §103 as unpatentable over Matsuo (US5312769) taken with Zamanian and Toshiyuki. This is a rejection that has been carried over from a previous Office Action. Applicants have previously addressed the shortcomings of this rejection and will repeat their arguments here. In a previous rejection, the Examiner asserted that Matsuo taught an overreaching step. The Examiner now concedes that Matsuo does **not** so teach.

Matsuo teaches forming transistors on a semiconductor substrate, and then forming polysilicon lead pads that are electrically connected to the transistors. An interlayer insulating film is formed over the transistors and lead pads. Bit lines are then electrically connected to the transistors and a second interlayer insulating film is formed over the bit lines. Contact holes are formed in the first interlayer insulating film to expose the lead pads. Polysilicon is then selectively grown on the surfaces of the exposed lead pads.

With respect to claim 21, that claim recites "forming an underlayer having an opening over the at least one semiconductor layer." Matsuo, to the contrary, describes word lines 102-104 having an insulating film 21 "formed around the word lines" (col. 4, lines 13-14). The Examiner asserted that insulating film 21 corresponds to the claimed underlayer. However, as shown in the figures, there is no "opening" in any of the insulating films 21. Such films form a continuous structure "around the word lines." If the Examiner is pointing to the areas *between* the word lines 102-104, then that structure fails to describe an underlayer having an opening therein. For these reasons, neither Matsuo, nor the secondary references, teach or suggest this claim limitation.

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The Examiner also concedes that "Matsuo fails to show etching in an overetch amount of the substantially vertical component." The Examiner has attempted to remedy this admitted deficiency in Matsuo by turning to Zamanian and Toshiyuki. However, Zamanian's conductive layer 32 of polysilicon is not etched at all. It is the barrier layer 34 that is etched. The teachings of Matsuo and Zamanian are not combinable in the manner proposed by the Examiner. Matsuo does not need a multi-layer "pad" that includes a barrier layer. And Zamanian fails to teach overetching of a conductive layer.

Toshiyuki shows a very different geometry for the formation of an interconnect structure. There is no motivation to use the technique of Toshiyuki to expose the very different polysilicon lead pads of Matsuo. The Examiner has failed to carry his burden of establishing, by evidence, a prima facie case for obviousness.

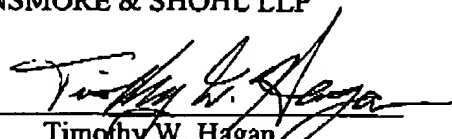
With respect to claim 31, as discussed above, no portion of Zamanian's conductive layer 32 has a contact hole etched therein. Nor does Toshiyuki teach or suggest a contact hole in an overlayer that extends into the vertical component of a layer of conductive material. The Examiner concedes that Matsuo also does not. Thus none of the cited references, either taken alone or together teach or suggest the claimed subject matter of claims 31-32. For all of these reasons, applicant submits that claims 21-25 and 31-32 as amended are patentable over Matsuo, Zamanian, and Toshiyuki.

For all of these reasons, applicants submit that claims 21-25 and 31-32, as amended, are patentable over the applied art of record. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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